THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte STEPHEN C. HORNE
and
SCOTT H.R. McMAHON

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Appeal No. 97-1784
Application 08/011,068[1]

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ON BRIEF

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Before THOMAS, FLEMING and CARMICHAEL, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

[1] Application for patent filed January 29, 1993.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 20, all of the claims pending in the present application.

The invention relates to a clock generation circuitry that provides clock signals with controlled duty cycles.

The independent claim 1 is reproduced as follows:

1. A digital clock waveform generator comprising:

a variable delay circuit including an input line, an output line, a propagation path coupled between said input line and said output line, and a control line, wherein said variable delay circuit is configured such that a propagation delay of said propagation path between said input line and said output line is variably controllable in response to a control signal provided to said control line;

a control unit coupled to the control line of said variable delay circuit and configured to iteratively adjust the propagation delay of said variable delay circuit such that a period of a timing signal provided to said input line of said variable delay circuit is coverged [sic, converged] upon by the propagation delay of said variable delay circuit; and

a signal synthesis circuit coupled to a node connected to the propagation path of said variable delay circuit, wherein said signal synthesis circuit is configured to generate a clock signal having a duty cycle and a period that are dependent upon signal transitions between a high logical state and a low logical state occurring at said node connected to the propagation path of said variable delay circuit.

The Examiner relies on the following references:

Collins et al. (Collins)	4,063,308	Dec. 13, 1977
Rubinstein	5,077,686	Dec. 31, 1991

Claims 1 through 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Rubinstein and Collins.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 20 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d

1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

In regard to the rejection of claims 1 through 7 and 12 through 20, Appellants argue that Rubinstein and Collins, together or individually, fail to teach or suggest iteratively adjusting the propagation delay of the variable delay circuit such that a period of a timing circuit is converged upon by the propagation delay of the variable delay circuit. The Examiner argues on page 5 of the answer that Collins teaches in column 4, lines 3 through 9, convergence of a timing signal.

Upon a careful review of Rubinstein and Collins, we find that neither reference teaches adjusting the propagation delay of a variable delay circuit to match the period of a timing signal. In column 2, line 60, through column 3, line 7, Collins teaches that Figure 1 is a block diagram of a clock measuring and tuning system. In particular, Collins teaches that the system provides automatic tuning of the clock signals at a particular

node in a particular path within a data processing system. The tuning is done by automatically adjusting the time of arrival of the clock at the selected node so as to correspond with a predetermined timing so that the clock should arrive at this point to initiate some desired function. The time of arrival of a clock pulse at a particular node can be controlled by selecting the amount of delay inserted into the particular clock line.

In column 3, line 44, through column 4, line 9, Collins teaches with reference to Figure 1 that the service system 10 initiates an oscillator 12 which provides timed clock pulses of a predetermined frequency. An output from the oscillator 12 is connected to a programmable delay chip 14. This unit is under the control of the service system 10 and provides the delay which is ordered by the service system. This delay is applied to the clock pulse from the oscillator 12 producing a delayed clock pulse which is then applied to various logic and array chips within the system being tuned. The delayed clock pulse is then applied to the time detector unit 20 where the delayed clock pulse is compared to a reference time pulse produced by a reference generator circuit 22. The results of the comparison is

provided to the service system 10 which responds by adjusting the delay introduced by the programmable delay chip 14 to thereby change the phase of the delayed clock pulse so that it will correspond with the generated reference time pulse.

In column 5, lines 1 through 26, Collins teaches that Figure 3 shows the block diagram of the programmable delay

chip 14. Upon a closer review of Collins, we find that Collins teaches that the programmable delay chip 14 is able to adjust the phase of the clock pulse and the phase is changed so as to bring the clock pulse in phase with a reference clock pulse. However, Collins does not teach adjusting the propagation delay of a variable delay circuit such that a period of a time signal is converged upon by the propagation delay of the variable delay circuit.

Appellants argue that one of ordinary skill in the art would have no motivation or incentive to modify Rubinstein and Collins so as to adjust the propagation delay of a variable delay circuit such that a period of a time signal is converged upon by the propagation delay of the variable delay circuit.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg.***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13. Upon reviewing Rubinstein and Collins, we fail to find any suggested desirability of modifying Rubinstein and Collins to obtain a digital clock wave form generator or a method for generating a clock signal as recited in Appellants' claims 1 through 7 and 12 through 20.

In regard to the rejection of claims 8 through 11, Appellants argue that Rubinstein and Collins, together or individually, fail to teach or suggest a lock window unit wherein the extent of propagation through the lock window circuit indicates the deviation of the propagation delay of the delay

chain from the period of the time signal. Appellants argue that the propagation through the lock window circuit measures the amount to adjust the delay elements so as to converge on the period of the time signal. Appellants argue that neither Rubinstein nor Collins teaches or suggests a lock window circuit as recited in claim 8.

On page 4 of the answer, the Examiner argues that Collins teaches a lock window circuit in column 5, lines 15-25. The Examiner argues that array 50 shown in Figure 3 meets Appellants' claimed lock window unit. On page 6, the Examiner further argues that Collins teaches in Figure 4 a lock window circuit.

Upon a closer reading of Collins, we find that Collins teaches in column 5, lines 5-24, a programmable delay chip 14 which is a variable length clock path whose delay is a function of the circuit technology and of the bit patterns stored in a 6x7 array 50. The array 50 is used to hold the bit patterns which in turn condition the paths through first and second sections 51 and 53, respectively, so as to vary the delay in each of the three delay adjustments gross, medium and fine. In column 5, line 43, through column 6, line 7, Collins teaches that Figure 4 shows the

gross adjust network 58 which provides the gross adjustments. However, we fail to find any teaching or suggestion of using a propagation through the lock window circuit to measure the amount of needed adjustments of the delay elements to converge on the period of the time signal. Furthermore, we fail to find that Rubinstein and Collins teach or suggest a digital clock wave-form generator comprising a delay chain, a lock window unit, a control unit and a clock synthesis circuit as recited in claims 8 through 11.

We have not sustained the rejection of claims 1 through 20 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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MICHAEL R. FLEMING	)	APPEALS AND
Administrative Patent Judge	)	INTERFERENCES
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